ABSTRACT OF THE DISCLOSURE

Embodiments of the invention include a memory controller to interface to memory. In one embodiment, the memory controller includes a pull-up calibration terminal to couple to an external pull-up resistor, a pull-down calibration terminal to couple to an external pull-down resistor, a voltage reference node, a first switch coupled between the pull-up calibration terminal and the voltage reference node, and a second switch coupled between the pull-down calibration terminal and the voltage reference node. The first switch and the second switch may be selectively closed to generate an internal voltage reference on the voltage reference node in a normal mode that may be used for comparison with an input signal to receive data.